IN THE UNITED STATES PATENT & TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: **ERIC ADLER**	§ § §	Attorney Docket No.: **BUR919990222US2**
Serial No.: **10/057,185**	§ § §	Examiner: **TUGBANG, A. DEXTER**
Filed: **JANUARY 25, 2002**	§ §	
Title: **METHOD OF FABRICATING A** **CAPACITOR HAVING SIDEWALL** **SPACER PROTECTING THE** **DIELECTRIC LAYER**	§ § § §	Group Art Unit: **3729**

APPEAL BRIEF

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Sir:

This Brief is submitted in triplicate in support of the Appeal in the above-identified application.

CERTIFICATE OF MAILING
37 C.F.R. § 1.8(a)

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Date: 3/15/04   By: _Brian F. Russell_
                            Signature

REAL PARTY IN INTEREST

International Business Machines Corporation, the assignee of record, is the real party in interest in the subject Appeal.

RELATED APPEALS AND INTERFERENCES

No appeals or interferences known to Appellant, Appellant's legal representative, or assignee will directly affect or be directly affected by or have a bearing on the Board's decision in the present Appeal.

STATUS OF THE CLAIMS

Claims 1-17 were originally presented in the present Application, with Claims 1-8 being canceled and Claims 17-20 being entered in the Preliminary Amendment filed concurrently with the Application on January 25, 2002. Claims 21-22 were subsequently entered in Amendment A, having a mailing date of June 11, 2003, but withdrawn from consideration by the Examiner in the Final Rejection dated August 27, 2003, and labeled Paper No. 7. A Supplemental Amendment filed September 30, 2003, was proposed pursuant to the Examiner's recommendation, but refused entry by the Examiner in the Advisory Action dated October 14, 2003, and labeled Paper No. 11. Claims 9-20 stand finally rejected by the Examiner as noted in the Advisory Action dated October 14, 2003, and labeled Paper No. 11. The rejection of each of Claims 9-20 is appealed.

STATUS OF AMENDMENTS

A Supplemental Amendment was proposed but not entered subsequent to the Final Rejection dated August 27, 2003, and labeled Paper No. 7.

SUMMARY OF THE INVENTION

As described in the present specification at page 2, line 10 *et seq.*, metal-insulator-metal (MIM) capacitors are commonly employed in analog integrated circuits. In the fabrication of MIM capacitors, the top and bottom plates are commonly defined by a single etching step. The present invention recognizes that this single etching step can lead to contamination at the edge of the dielectric layer that contacts both plates. This contamination can cause undesirable leakage between

the top and bottom capacitor plates. Accordingly, the present invention is directed to a method of fabricating a capacitor that protects the dielectric layer from contamination during the etch process utilizing one or more sidewall spacers.

An exemplary method of fabricating a capacitor in accordance with the present invention is described at page 10, line 8 *et seq.* and depicted in the flowchart given in Figure 8. The illustrated method begins at block 160 and thereafter proceeds to block 162, which illustrates the formation of metal damascene conductors 20, 21 in semiconductor substrate 10. Next, at block 164, Si_3N_4 layer 30 is formed over substrate is 10, and an opening is etched in Si_3N_4 layer 30. If overetching of metal damascene conductors 20-21 is not a concern, then block 164 can optionally be omitted. The resulting structure is illustrated in Figure 1.

Referring again to Figure 8 and page 10, line 18 *et seq.* of the specification, a first barrier layer 40 is then added at block 166 that contacts metal damascene conductor 20. At block 168, the remainder of the MIM capacitor structure is formed by sequentially forming bottom electrode 50, second barrier layer 60, dielectric layer 70, third barrier layer 80, top electrode 90 and fourth barrier layer 100. In addition, an overlying insulator layer 110 may optionally be formed in order to retard charge leakage. The resulting structure is depicted in Figure 2.

Thereafter, as depicted at block 170 of Figure 8 and described at page 10, line 27 *et seq.* of the specification, a photo mask 120 is utilized to pattern capacitor top plate (e.g., layers 80, 90 and 100) in an etch back of the capacitor 30 stack stopping on dielectric layer 70. The structure resulting from the etch back is depicted in Figure 3. Next, as shown at block 172, one or more sidewall spacers 132 are formed around the perimeter of the top plate and over dielectric layer 70 through the deposition and etching of silicon dioxide, for example. The formation of sidewall spacers 132 is illustrated in Figures 4 and 5. Sidewall spacers 132 protect dielectric layer 70 from overetching and contamination 5 during the subsequent etch of dielectric layer 70 and the bottom plate (e.g., layers 40, 50 and 60), which is depicted at block 174 of Figure 8 and in Figure 6. The etch of the bottom plate stops on silicon nitride layer 30, if present.

As described in the present specification at page 11, line 10 *et seq.*, after the essential structure of the capacitor has been defined by the foregoing etching steps, capacitor fabrication continues at block 176 of Figure 8, which depicts forming silicon nitride layer 134 on the top and sides of the capacitor stack and depositing and planarizing interlayer dielectric 136. Finally, as illustrated at block 178, contacts 150 to the top plate and metal damascene conductor 21 are formed, and wiring 140 is deposited in a conventional manner. Thereafter, the process ends at block 180, with the fully formed MIM capacitor shown in Figure 7.

By forming a capacitor in accordance with this method, the dielectric layer (e.g., dielectric layer 70) is protected from contamination during the etch process, preventing undesirable leakage between the capacitor plates.

ISSUES

(1) Is the Examiner's rejection of Claims 9 and 14-19 under 35 U.S.C. § 102(b) as unpatentable over U.S. Patent No. 5,742,472 to *Lee et al.* (*Lee*) well-founded?

(2) Is the Examiner's rejection of Claim 10 under 35 U.S.C. § 103(a) as unpatentable over *Lee* in view of U.S. Patent No. 4,172,758 to *Bailey et al.* (*Bailey*) well-founded?

(3) Is the Examiner's rejection of Claims 11-13 and 20 under 35 U.S.C. § 103(a) as unpatentable over *Lee* in view of U.S. Patent No. 5,795,819 to *Mostiff et al.* (*Mostiff*) well-founded?

Given the grouping of the claims set forth below, the resolution of the first issue will, for purposes of the present appeal, necessarily resolve the second and third issues.

GROUPING OF THE CLAIMS

For purposes of this Appeal, all claims stand or fall together as a single group.

ARGUMENT

I.   Introduction

Claims 9 and 14-19 stand finally rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,742,472 to *Lee et al.* (*Lee*). That rejection is not well founded and should be reversed.

II.   *Lee* does not teach or suggest each feature of exemplary Claim 9

Lee does not render exemplary Claim 9 unpatentable because the cited reference does not teach or suggest the combination of features recited in exemplary Claim 9. In particular, the cited prior art references do not teach or suggest, "A method of fabricating a capacitor structure on a semiconductor substrate ... comprising ... forming at least one insulating sidewall spacer placed against said perimeter of said top plate and <u>overlaying</u> a portion of said dielectric layer" (emphasis supplied), as recited in exemplary Claim 9.

With respect to this feature, the Examiner, at page 4 of the Final Rejection dated August 27, 2003, and labeled Paper No. 7, cites *Lee's* sidewall spacers 70 shown in Figures 4-6. However, it is evident from the above-noted figures of *Lee* that sidewall spacers 70 do not <u>overlay</u> a portion of dielectric layer 30, as that term is commonly understood in the art. The Examiner seeks to dismiss this omission of *Lee* by attempting to equate the word <u>overlaying</u> with the word <u>against</u> (viz. "forming insulating sidewall spacers 70 ... **against or overlaying** a portion, i.e. outer perimeter, of the dielectric layer 30" (Final Rejection, page 4, lines 5-7, emphasis supplied)). Appellant respectfully traverses the Examiner's position for the reasons set forth below.

A.   Claim term must be given broadest reasonable interpretation as interpreted within the field of the invention by those of ordinary skill in the art

In order to properly construe claim terminology during examination, including the term <u>overlaying</u> as employed in Claim 9, the proper standard of claim construction must first be adopted. MPEP 2111 sets forth that standard as follows: "During patent examination, the pending claims must be 'given their broadest reasonable interpretation consistent with the specification.' *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000)." This standard is further elucidated in MPEP 2111.01, which states: "When not defined by applicant in the specification, the words of a

claim must be given their plain meaning ... as they would be interpreted by those of ordinary skill in the art. *Rexnord Corp. v. Laitram Corp.*, 274 F.3d 1336, 1342, 60 USPQ2d 1851, 1854 (Fed. Cir. 2001)." See also, *Toro Co. v. White Consol. Indus., Inc.*, 199 F. 3d 1295, 1299, 53 USPQ2d 1065, 1067 (Fed. Cir. 1999)("[W]ords in patent claims are given their ordinary meaning in the usage of the field of the invention ..."). By synthesizing the foregoing citations from the MPEP, it is evident that the appropriate standard for claim construction during examination is that a claim term not defined in the specification must be (1) given its broadest reasonable interpretation (2) consistent with the specification (3) as that claim term would be understood by those having ordinary skill in the art (4) as used within the field of the invention.

B.   The term "overlaying" in exemplary Claim 9 refers to the vertical superposition of a layer over a previously formed layer with respect to the underlying substrate

Turning now specifically to an evaluation of the individual components of the above-cited standard of claim interpretation, Appellant first notes that page 1, lines 20-22 of the present specification state that the technical field of the invention is integrated circuit fabrication. This statement of the field of the invention is further supported by the remainder of the present specification, which describes in detail the steps involved in the fabrication of a capacitor on a semiconductor substrate. Accordingly, the field of the invention for the purpose of construing the term overlaying is the field of integrated circuit or semiconductor fabrication, and a person of ordinary skill in the art for purposes of the present invention is a person of ordinary skill in the art of semiconductor or integrated circuit fabrication.

Next, with respect to the "ordinary meaning" of the term overlaying as understood by those skilled in the art of semiconductor or integrated circuit fabrication, Appellant submits herewith a number of references in Appendix B demonstrating the use of the related term overlay. Specifically, in Ruzyllo, J., *Semiconductor Glossary*, 2001 (accessed at www.semiconductorglossary.com, 9/12/2003), the term overlay is defined as the "superposition of the pattern on the mask to the pattern previously created on the surface of the wafer." In other words, overlay refers to a layer vertically stacked upon another layer over the surface of a wafer by a semiconductor processing step. This understanding is confirmed by the two additional references submitted in Appendix B (Sullivan, N.,

"Fundamentals of Overlay Metrology," *Semiconductor International*, 9/1/2001 and "Micro-Metric launches Innova 200," www.compoundsemiconductor.net, 7/29/2003), which discuss overlay metrology, that is, the measurement of overlay alignment errors. Both of these additional references disclose "the difference between the two centerlines (in X and Y directions) [of the overlay patterns] constitutes an overlay measurement" ("Micro-Metric launches Innova 200," paragraph 2). Because overlay alignment measurements are taken in the X and Y directions (i.e., the Cartesian coordinate system axes parallel to the plane of the semiconductor substrate), it is clear that the overlays themselves are stacked along the Z or vertical axis with respect to the semiconductor substrate. Hence, the ordinary meaning of the term <u>overlaying</u> to those skilled in the art of semiconductor or integrated circuit fabrication must be taken to mean the vertical superposition of an overlay over a previously formed layer with respect to the underlying substrate.

This meaning is entirely consistent with respect to the usage of the term <u>overlaying</u> in the present claims and in the specification as a whole. It should first be noted that Claim 9 recites the term <u>over</u> or <u>overlaying</u> four different times. That is, Claim 9 recites the steps of "forming a metallic bottom plate <u>over</u> the semiconductor substrate;" "forming a dielectric later <u>overlaying</u> the bottom plate;" "forming <u>over</u> the dielectric layer a top plate ...;" and "forming at least one insulating sidewall spacer ... <u>overlaying</u> a portion of said dielectric layer." In each case, it is clear from the claim and the corresponding drawings and description in the specification that vertical superposition with respect to the substrate is in mind. Also, it should be noted that except for the last use of the term <u>overlaying</u>, the Examiner construes <u>over</u> or <u>overlaying</u> to refer to the vertical stacking of layers, citing vertically stacked layers in Figures 4-6 of *Lee*. With respect to the last usage of the term <u>overlaying</u> in Claim 9, however, the Examiner, based upon the disclosure of *Lee*, seeks to distort the meaning of <u>overlaying</u> to include other physical relationships, including that denoted by the term <u>against</u>.

C.   The Examiner's proposed construction of "overlaying" is erroneous

The Examiner's proposed interpretation of <u>overlaying</u> as meaning <u>against</u> is manifestly incorrect in that it is not supported by the present specification or any citation to a reference showing how the term <u>overlaying</u> would be understood by those skilled in the art. The Examiner's only

citation regarding the meaning of the term <u>overlaying</u> is to the American Heritage Dictionary, a non-technical reference which defines the term <u>overlaying</u> as "to lay or spread over or on" (Page 2 of Advisory Action dated September 30, 2003, labeled Paper No. 9). In making this citation the Examiner has not documented any consideration of whom he regards as a person of ordinary skill in the art or demonstrated that those skilled in the art would repair to the American Heritage Dictionary to define technical terms in their art. Moreover, Appellant notes that the Examiner's own proposed definition does not include the term <u>against</u>, which is urged by Examiner as equivalent to or encompassed by <u>overlaying</u>.

III. Conclusion

In view of the Examiner's incorrect construction of the term <u>overlaying</u>, which is the foundation of the § 102 rejection of exemplary Claim 9 in view of *Lee*, Appellant respectfully requests that the Board reverse the rejection of exemplary Claim 9 and all claims dependent therefrom.

Enclosed is a check in the amount of $110.00 for a one-month extension of time. Please charge IBM Corporation Deposit Account No. **09-0456** in the amount of $330.00 for submission of a Brief in Support of Appeal. No additional fee is believed to be required; however, in the event an additional fee is required please charge that fee to Deposit Account No. **09-0456**.

Respectfully submitted,

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ATTORNEY FOR APPELLANT

1.-8. (canceled)

9.   A method of fabricating a capacitor structure on a semiconductor substrate, said method comprising:

forming a metallic bottom plate over the semiconductor substrate;

forming a dielectric layer overlaying the bottom plate;

forming over the dielectric layer a top plate having a smaller area than said bottom plate, said top plate having a perimeter; and

forming at least one insulating sidewall spacer placed against said perimeter of said top plate and overlaying a portion of said dielectric layer.

10.   The method of Claim 9, and further comprising:

prior to forming said at least one insulating sidewall spacer, etching said top plate to expose said dielectric at said perimeter of said top plate.

11.   The method of Claim 9, wherein:

said method further comprises forming a conductor embedded in a the semiconductor substrate; and

forming the bottom plate comprises forming the bottom plate overlaying and in electrical contact with the conductor.

12.   The method of Claim 11, wherein forming a conductor comprises forming a copper damascene structure.

13.   The method of Claim 11, wherein forming said bottom plate comprises forming a conductive barrier layer in contact with said conductor.

14.   The method of Claim 9, wherein said step of forming a top plate comprises forming a metallic plate.

15.   The method of Claim 9, wherein forming the dielectric layer comprises forming a silicon dioxide layer.

16.   The method of Claim 9, and further comprising forming an insulating cap overlaying said top plate.

17.   The method of Claim 16, wherein said insulating cap has a perimeter coextensive with said top plate, and wherein forming said at least one insulating sidewall spacer comprising forming said at least one insulating sidewall spacer against said perimeter of said insulating cap.

18.   The method of Claim 9, wherein forming at least one insulating sidewall spacer comprises forming at least one insulating sidewall spacer on a top surface of the dielectric layer.

19.   The method of Claim 18, wherein forming at least one insulating sidewall spacer comprises forming at least one insulating sidewall spacer overlaying a portion of said bottom plate.

20.   The method of Claim 9, and further comprising:

forming a copper damascene conductor in a the semiconductor substrate underlying said bottom plate.

21.   The method of Claim 9, and further comprising forming an etch stop layer overlaying said semiconductor substrate prior to forming said bottom plate, wherein at least a portion of said bottom plate overlays said etch stop layer.

22.   The method of Claim 16, and further comprising forming a conductive via through said insulating cap and in electrical contact with said top plate.
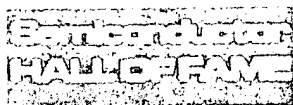
APPENDIX B

Semiconductor Glossa

Semiconductor OneSource

Copyright Jerzy Ruzyllo, 2001

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Search For Term:

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OneSource HOME

SEMICONDUCTOR HANDBOOK

Term (Index)	Definition
overlay	superposition of the pattern on the mask to the pattern previously created on the surface of the wafer.
alignment	positioning of the mask (or reticle) in lithographic processes relative to a wafer prior to exposure of the resist.

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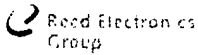
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The Fundamentals of Overlay Metrology

Neal T. Sullivan, Technology Development Group, Schlumberger ATE/VS, Concord, Mass. -- *Semiconductor International*, 9/1/2001
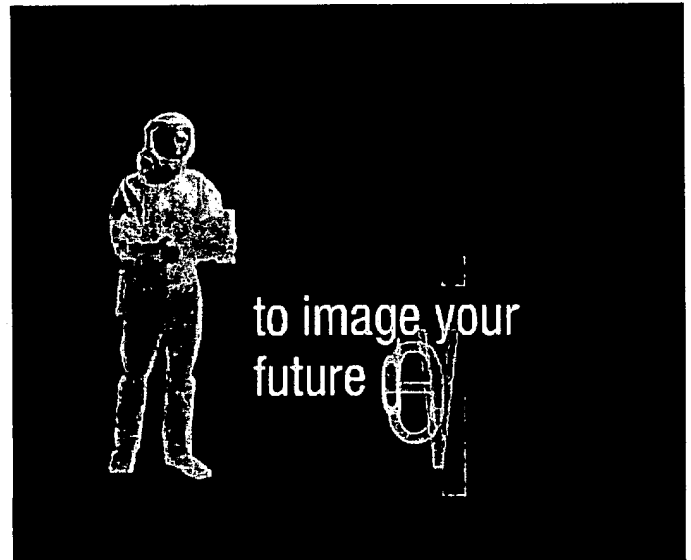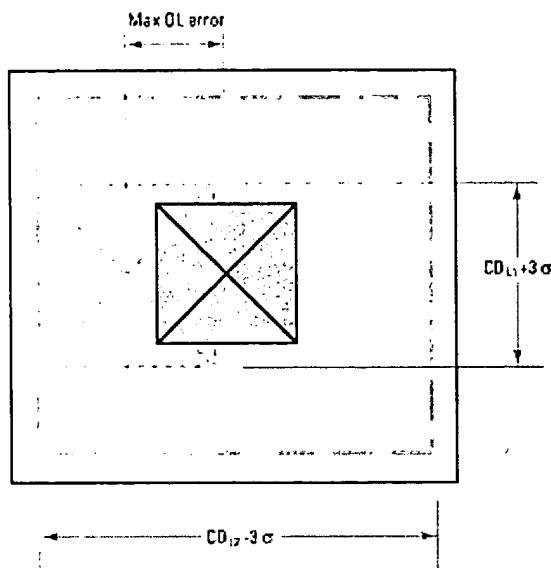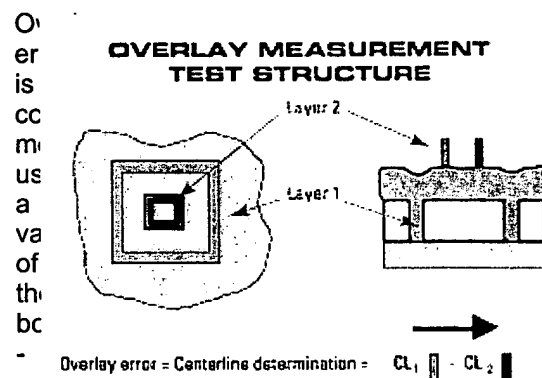
Overlay metrology equipment historically has had little difficulty meeting state-of-the-art process error budgets through the 0.25 µm technology node. In fact, typical overlay measurement equipment performance has been better than metrology error budget allocations by 20-30%.[1] This can be ascribed to several factors. First is the lavish error budget, compared with critical dimension (CD) metrology (3% of minimum design rule vs. <1% for CD metrology). The second is the relative stability of the overlay measurement target design, which typically doesn't scale (in the wafer plane) with each process generation, thereby presenting similar measurement issues for each successive process generation.

At a Glance

An overview of the basics of overlay metrology, including process and measurement error sources.

Finally, this historic ease of meeting process error tolerance can also be attributed to the lack of a clear connection to device yield. For CD measurements, clear relations to circuit performance and cost are used to derive specific process control limits.[2] In the case of overlay metrology, the correlation to final device yield is a much more complex combination of factors and, as such, is much more difficult to determine.

Semiconductor pattern overlay is the measure of vector displacement from one process level (substrate) to another level (resist), usually separated by an intermediate (thin-film) layer. The overlay requirements for a particular device design are typically determined through a combination of CD and overlay excursions.

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This is shown schematically in Figure 1, where

DESIGN RULE GENERATION SCHEMATIC

Max OL error

$CD_{L1} + 3\sigma$

$CD_{L2} - 3\sigma$

1. The maximum allowable overlay shift shown as the center-to-center distance.

the shaded square represents one level and the open square represents the second level.[3] In this example, the level-one critical dimension (CD_{L1}) is increased by the maximum tolerance (3σ), and the level-two critical dimension (CD_{L2}) is reduced by the maximum tolerance (3σ). The maximum allowable overlay shift, while maintaining level one (dark box) completely within level two (light box) — the design rule for this example — is shown as the center-to-center distance.

Overlay is commonly used as a variety of the bo

OVERLAY MEASUREMENT TEST STRUCTURE

Layer 2

Layer 1

Overlay error = Centerline determination = $CL_1 - CL_2$

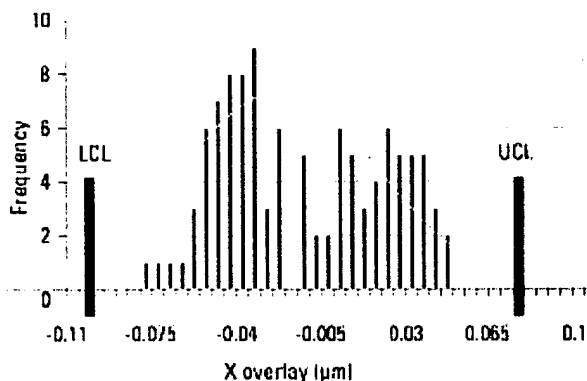**2. A box-in-box test structure is commonly used to measure overlay error.**

in-box test structure (Fig. 2) and is defined as the planar distance from the center of the substrate target (outer green box) to the center of the resist defined target (inner blue box). Overlay measurement involves the determination of the centerline of each structure along both the X and Y axes. Centerline determination utilizes the symmetry around the structure's center such that the error associated with edge determination will tend to cancel from each side of the structure. Conversely, in a linewidth determination, the error associated with each edge combines in an additive fashion.

PLATYKURTIC OVERLAY DISTRIBUTION

3. A typical example of the non-normal nature of the raw overlay measurement results.

Overlay measurement uncertainty is a complex function of tool, target and process interactions, and is difficult to quantify. The device overlay tolerance specification is derived from the technology design rules. The circuit performance requirements are compared with established manufacturing tolerances. All error sources — from the mask to the measurement uncertainty — are combined either linearly (most conservative) or are added in quadrature (for Gaussian error distributions) to calculate the overlay tolerance. Successful process control of 0.35 µm process technology was possible through initial stepper/scanner matching and subsequent control of layer-to-layer overlay through the use of X and Y offsets. Process tolerances for the 0.35 µm generation, typically 100 nm on critical levels, were generous enough that the non-normal (multi-modal) behavior and dependence on location within a field did not affect the ability to meet target performance specifications. A typical example of the non-normal nature of the raw overlay measurement results is shown in Figure 3. It is readily apparent from the figure that the actual data distribution is multi-modal and platykurtic.[4] This form of the data distribution is due to systematic lithography errors.

Product misregistration overlay budgets for current 0.18 µm production process technologies, however, are <70 nm. To consistently achieve these levels of performance, every aspect of overlay error must be identified and corrected. To that end, modeling is employed to correct the systematic

sources of overlay error. Process control is more difficult unless these systematic errors can be accounted for, because their presence distorts the observed nature of the variation.

Process error sources

The sources of overlay error attributable to the wafer stepper/scanner generally arise from the lens (intrafield) and the stage (grid). Intrafield errors can be further broken out into errors that either are intrinsic to the optics of the stepper/scanner (distortions) or are derived from interactions of the reticle with the stepper/scanner's optical subsystem.

The former set of errors are characteristic of a given lens and are typically addressed during lens manufacture (direct control over a wafer stepper/scanner to control intrinsic lens distortions is not available). The residual lens distortions are accommodated for, at the price of individual stepper/scanner overlay performance, in the process of stepper/scanner matching. Therefore, it is essential that each new lens be thoroughly characterized with respect to distortion because these errors are an integral part of the performance of the stepper/scanner in manufacturing.

Equation 1 is a mathematical model for all X direction intrafield error terms associated with stepper (a similar equation applies for the Y direction).[5]

$$\delta x = a + (\delta M/M)x_0 - \theta y_0 - t_1 x_0{}^2 - t_2 x_0 y_0 - (1)$$

$$Ex_0(x_0{}^2 + y_0{}^2) + Fx_0(x_0{}^2 + y_0{}^2)^2 + \text{Residuals}$$

From Equation 1, the terms up to first order in x — offset (a), magnification ($\delta M/M$) and rotation (θ) — can typically be controlled from the stepper/scanner. The higher-order terms, trapezoid (t_1 and t_2), third (E) and fifth (F) order distortions are not easily controlled (trapezoid) or are intrinsic to the stepper lens (third and fifth order).

Stage-derived errors may also be divided into those over which the process engineer has control and those that are intrinsic to the mechanical subsystem. As shown in Equation 2, the systematic grid errors are very similar in mathematical form to the intrafield or lens errors shown in Equation 1.[6] But, unlike the intrafield case, the terms apply across the entire wafer.

$$\delta x = a + (\delta M_g/M_g)x_0 - \theta_g y_0 + y_0{}^2 Dx +$$

Residuals (2)

$\delta M_g/M_g$ is the wafer scaling coefficient, U_g is the wafer rotation coefficient and D is the stage bow coefficient.

Typically, the stepper will allow direct control over only the scale and rotation terms. Accurate separation of the various error components shown in Equations 1 and 2 is heavily dependent upon both sample plan and model statistics. When establishing the metrology sample plan, it is important to maximize symmetry and spatial coverage. These concepts derive from an understanding of the systematic error components due to the lithography tool. To achieve symmetry, die and intrafield site positions should be chosen so that they are balanced by an opposite die or site (not necessarily within the same field location). For good spatial coverage, measurement locations must be positioned such that they adequately cover the area of interest (wafer or die) in both the X and Y directions. Poor symmetry can lead to incorrect systematic error assessment.

In the extreme intrafield case — one site per field — magnification error will appear as a translation error. Correction of this through an offset term will result in a 2× error at opposing die locations. Poor spatial coverage will also lead to incorrect systematic error assessment. For example, sampling the field in the four corners only will result in exaggerated field magnification terms. This is due to the

inclusion of (non-correctable) higher-order (third and fifth) distortion terms. In this instance, adding one or two sites along the die edge (at X=max, Y=0 or X=0, Y=max) will allow for differentiation of the higher-order systematic errors from magnification terms.

Error sources

Overlay measurement must be sensitive enough to discriminate error components derived from all sources. So it is critical that the contribution of the measurement tool to the total error be minimized and well controlled for all process levels.

Overlay measurement difficulties arise in manufacturing from an interaction of the measurement equipment with the instance of the measurement feature (process variations and target design), primarily due to low edge contrast. Low-contrast edges often result from advanced planarization techniques such as chemical mechanical polishing (CMP), used to accommodate a decreasing photolithography process window. These problems require that implementation of overlay metrology be performed with a deeper understanding of the physics of the measurement instrument and the interaction of the process module with the overlay measurement target. In effect, the sample must be considered to be an optical element of the measurement system.

The inherent, tool-limited measurement accuracy is commonly referred to as tool-induced shift (TIS).[7] TIS is quantified by measuring the same feature at 0 and 180° (wafer) rotations. TIS is half the sum of the measurements from each orientation. TIS error arises from optical alignment, illumination and aberrations of the system optics. TIS interacts with process conditions, achieving different values for different resist thicknesses, substrate surface roughness, substrate topographies and structure designs.[8]

While it is generally true that minimum TIS results in best overall metrology performance, it is also clear that there is a complex interaction between the various measurement schemes (optics, algorithms, illumination, etc.) and TIS performance on a given substrate. TIS is a very complex function of choice of focus method (e.g. single vs. double grab), optical configuration, and substrate material. It is not possible to accurately predict the TIS response for a given instrument on a new substrate based only on an empirical understanding of the instrument's performance on other materials.

Overlay measurement accuracy errors, if not recognized and accounted for, can produce false systematic stepper/scanner errors. The introduction of systematic measurement errors into a simulated stepper setup data set results in the transposition of those errors to the stepper.[9] TIS shows up in the translation term of the modeled stepper systematic errors, and pixel scale directly modifies the grid and field magnification (scale) coefficients. If these errors are not properly ascribed to the metrology tool, they will end up as a stepper/scanner input correction, which will further degrade product overlay performance. It is important to accurately quantify and assign the contribution of the measurement tool's error component to the measured value, and to minimize its impact via a hardware modification (e.g. optical alignment/columnation) or software calibration.

The final component of the measurement contribution to the overlay error comes from the measurement precision of the tool. This component is easily quantified by performing repeated measurements of a sample in a carefully designed analysis of variance experiment. All of these sources of measurement error combine to constitute the total measurement uncertainty.

This is an excerpt of an article that appeared in AIP Conf. Proc. 550, Characterization and Metrology for ULSI Technology, Eds: D.G. Sieiler, et al. Copyright American Institute of Physics, 2001. "Critical Issues in Overlay Metrology" appears on p. 346-356.

Author Information

Neal Sullivan is a technical adviser at Schlumberger's Verification Systems Division, working on development of next-generation metrology equipment. He has a B.S. in physics and philosophy from Boston College and an M.S. in solid-state physics from Purdue University.

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1. N. Sullivan, J. Shin, "Overlay Metrology: The Random, the Systematic and the Ugly,"*AIP Conference Proceedings,* Vol. 449, 1998, p. 143.
2. C.P. Ausschnitt, M.E. Lagus, "Seeing the Forest for the Trees: A New Approach to CD Control," *Proc. SPIE,* Vol. 3332, 1998, p. 212.
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4. Platykurtic distributions have little data in the tail regions and are characterized by a value of kurtosis which is less than zero.
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Product Release

Micro-Metric launches Innova 200

Date announced: 29 Jul 2003

Micro-Metric has a new, exceptionally accurate system for automated semiconductor overlay and linewidth measurement. Based on the company?s extensive background in precision dimensional metrology, the Innova 200 is a cost-effective solution to verify the alignment between layers on shrinking wafer geometries.

Innova 200 is unique in that it measures both linewidth and overlay dimensions, making it particularly effective in determining overlay alignment. The system creates an intensity profile of the overlay pattern in X and Y directions. Any pair of edges in the profile can be measurement targets. The centerline between these two measurement targets is determined for both the inner box and outer box; the difference between the two centerlines (in X and Y directions) constitutes the overlay measurement.

INNOVA 200 offers several important features:

Automatic wafer handler with prealigner, motorized nosepiece, and pattern recognition. Wafers can be loaded from and returned to any slot in either of two cassettes. The prealigner can align to flats of all sizes, or notches. The system automatically deletes alignment marks, and performs measurements without operator assistance

User-definable operating software: application programs included with Innova 200 are written using Micro-Metric?s powerful Measurement Control Language (MCL). Program files are easy to read, and allow users to modify existing programs to control the system.

Statistical data analysis: Innova 200 processes measurement results to determine the average, maximum, minimum, spread, standard deviation, and other statistical results from selected sets of data. Results are displayed on screen, printed as reports, saved to a file, or transferred directly to a statistical database.

Overlay measurement accuracy is 0.005 microns or less. Overlay measurement repeatability is 0.005 microns or less at 3 Sigma. Positioning resolution is 0.01 microns (10 nm). Velocity is 75 mm/sec. (3 in./sec.).

Innova 200 also measures a wide range of critical dimensions on wafers, such as linewidths, contacts, vias, circles, arcs, and other features ranging from 0.5 to 800 microns. The system can also be operated manually.

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